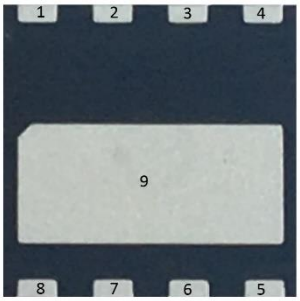
650V Enhancement-Mode GaN Power Transistor

Description

The series of devices are enhancement mode GaN on silicon power transistors. The properties of GaN allow for high voltage breakdown and high switching frequency. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g, offer improved efficiency over silicon power transistor.

Features

- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Qualified for standard grade applications according to JEDEC



Application

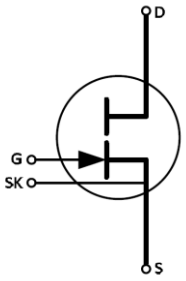
- High Voltage AC/DC conversion
- High Voltage DC/DC conversion
- High performance power supplies

1,2,3,4	Drain
5,6,9	Source
7	Kelvin Source
8	Gate

Key performance Parameters at T_j=25 ℃

Paremeter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(ON),typ}$	170	mΩ
$Q_{G,typ}$	2.0	nC
I_D	13	A
Q_{rr}	0	nC

Schematic Diagram



Package Marking and Ordering Information

Device	Package	Quantity
CGL65R190B	PQFN	

Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	-10 to +7	V
Continuous Drain Current	I_D	13	A
Continuous Drain Current(T_c=100 ℃)		8	A
Pulse Drain Current(Pulse width 300μs)	I_{DM}	20	A
Operating Junction Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.5	℃/W
Thermal Resistance, Junction-to-Ambient [a]	$R_{\theta JA}$	62	℃/W
Reflow soldering temperature, MSL3	T_{sold}	260	℃

Note：

a. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board

Electrical Characteristics (T_C=25℃ unless otherwise noted)

Static Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}		650	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V,V_{GS}=0V,T_j=25ºC	--	2	20	μA
Gate-body Leakage Current	I_{GSS}	V_{GS}=6V,V_{DS}=0V	--	--	200	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=5mA	0.95	--	1.50	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=6V, I_D=5A,T_J=25 ℃	--	170	190	mΩ
		V_{GS}=6V, I_D=5A,T_J=150 ℃	--	390	--	

Dynamic Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Capacitance	C_{iss}	V_{DS}=400V,V_{GS}=0V, f=1.0MHz		74		pF
Output Capacitance	C_{oss}			24		pF
Reverse Transfer Capacitance	C_{rss}			0.36		pF
Output Capacitance, energy related[1]	$C_{o(er)}$	V_{GS}=0,V_{DS}=0-400V		28		pF
Output Capacitance, time related[2]	$C_{o(tr)}$			37		pF
Output Charge	Q_{oss}			15		nC
Gate Resistance	R_g			1.0		Ω
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=400V,I_D=5A V_{GS}=0-6V,R_{on}=10Ω, R_{off}=3Ω, See Fig 17.		12		nS
Turn-on Rise Time	t_r			7		nS
Turn-Off Delay Time	$t_{d(off)}$			11		nS
Turn-Off Fall Time	t_f			9		nS

Gate Charge Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Total Gate Charge	Q_g	V_{DS}=400V,I_D=5A, V_{GS}=6V		2.0		nC
Gate-Source Charge	Q_{gs}			0.39		nC
Gate-Drain Charge	Q_{gd}			0.67		nC

Reverse Diode Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D=3A	---	2.5	---	V
Reverse Recovery Charge	Q_{rr}			0		nC

Note：1. Co(er) is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

2. Co(tr) is a fixed capacitance that gives the same charge time as C_{oss} while V_{DS} is rising from 0 to 400V

Typical Electrical and Thermal Characteristics

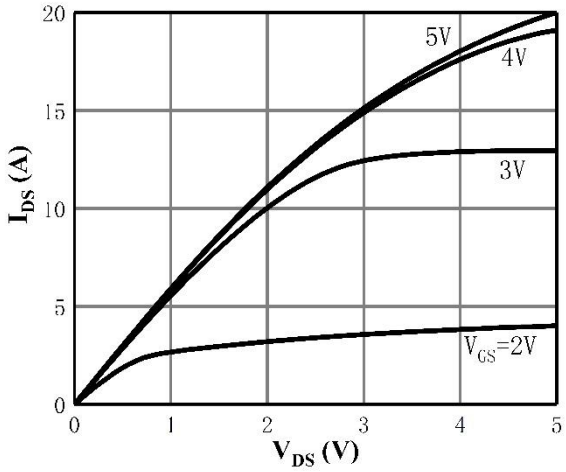


Figure 1. Output Characteristics at 25 ℃

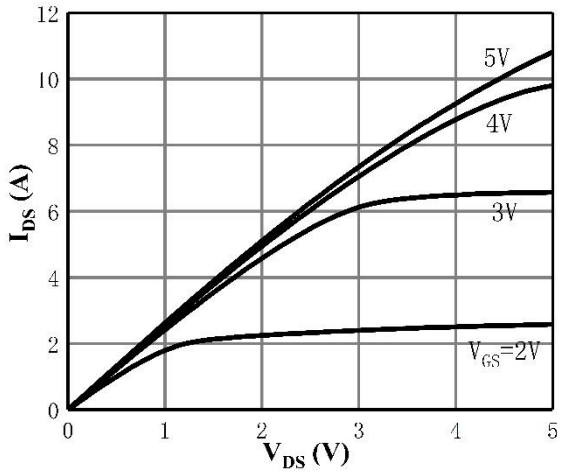


Figure 2. Output Characteristics at 150 ℃

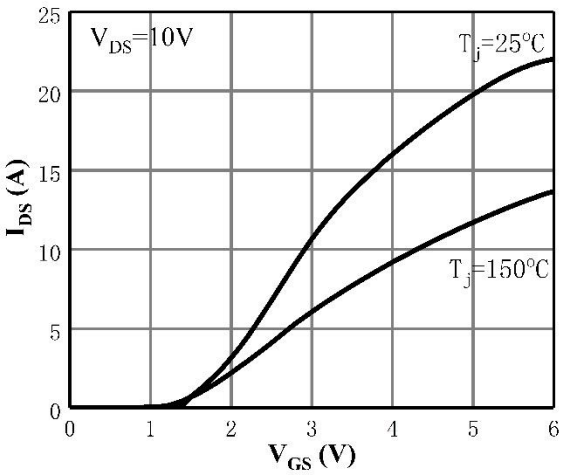


Figure 3. Transfer Characteristics

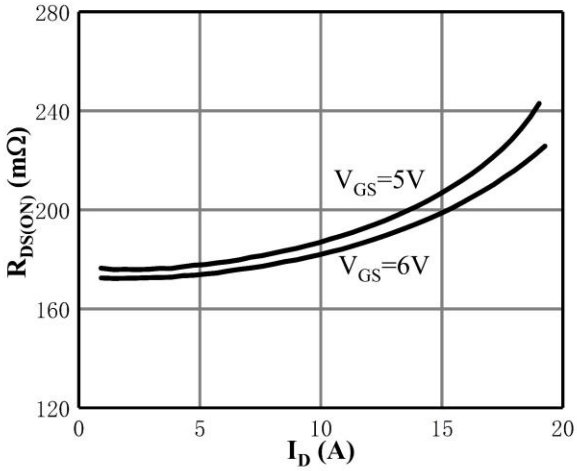


Figure 4. $R_{DS(on)}$-Drain Current

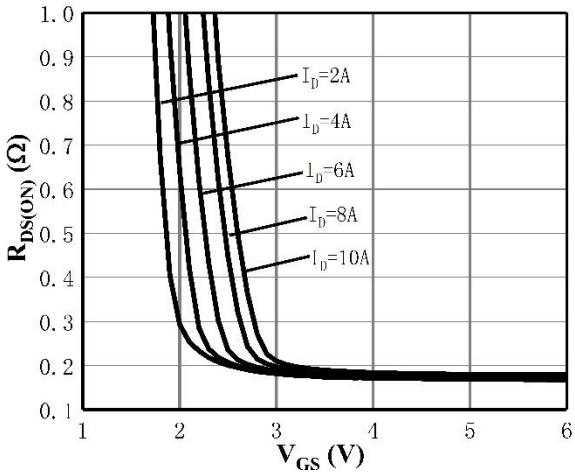


Figure 5. $R_{DS(on)}$-Gate Voltage at 25 ℃

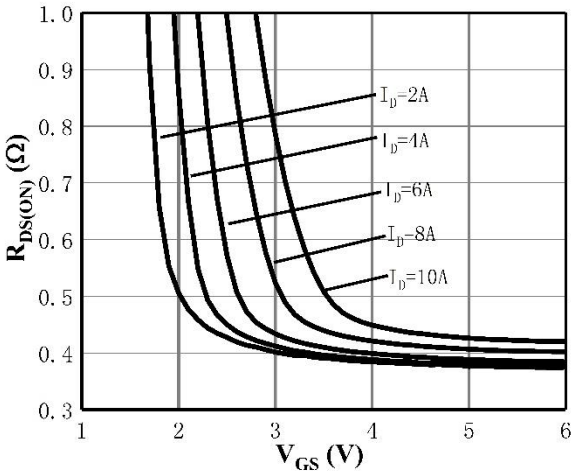


Figure 6. $R_{DS(on)}$-Gate Voltage at 150 ℃

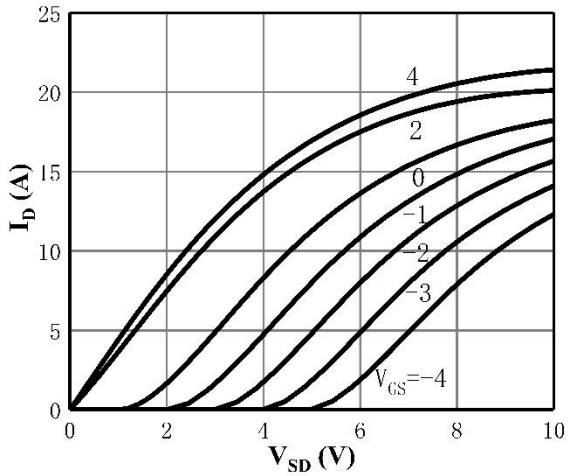


Figure 7. Reverse Characteristics at 25 ℃

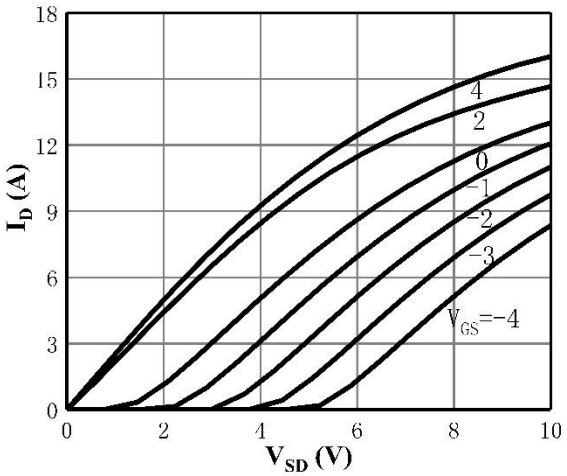


Figure 8. Reverse Characteristics at 150 ℃

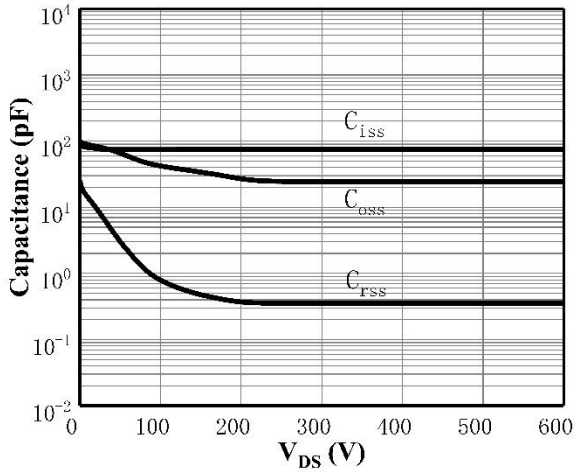


Figure 9. Capacitance vs V_{DS}

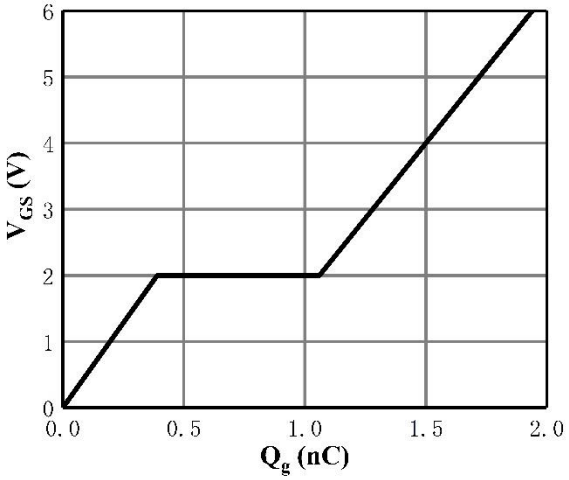


Figure 10. Gate Charge

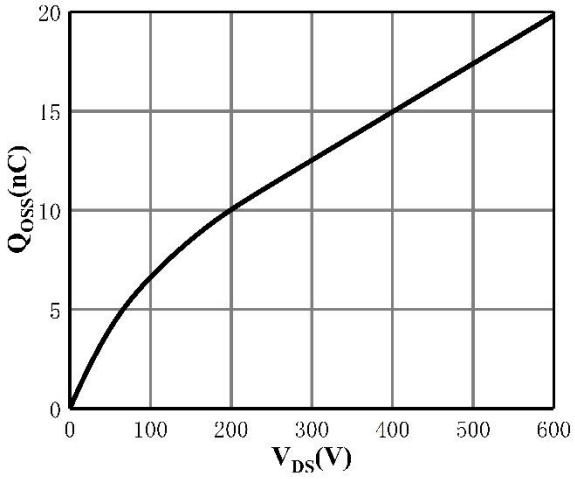


Figure 11. Output Charge

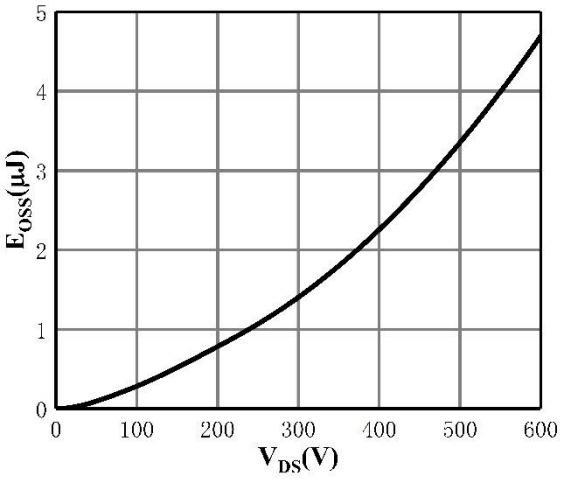


Figure 12. C_{OSS} Store Energy

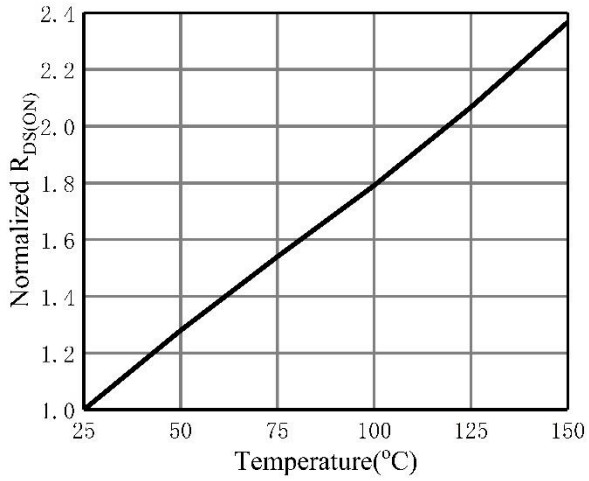


Figure 13. Normalized $R_{DS(ON)}$ vs T_J

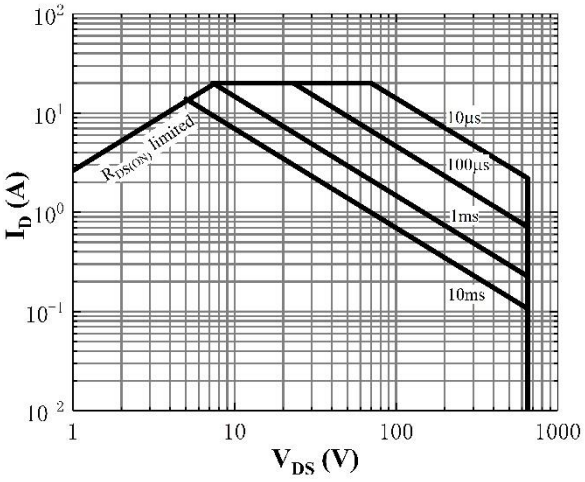


Figure 14. Safe Operating Area

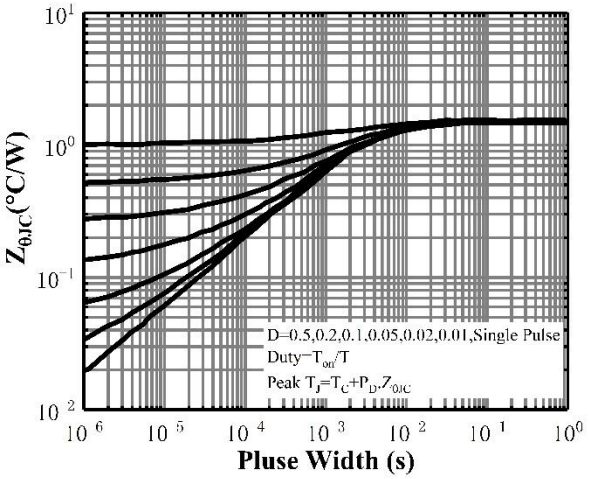


Figure 15. Transient Thermal Resistance

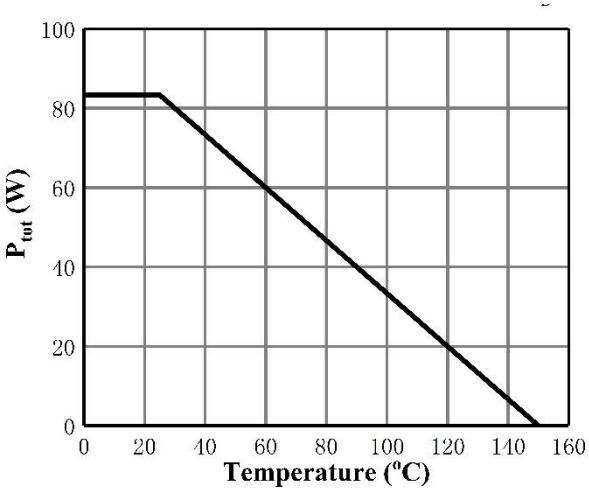


Figure 16.Power Dissipation

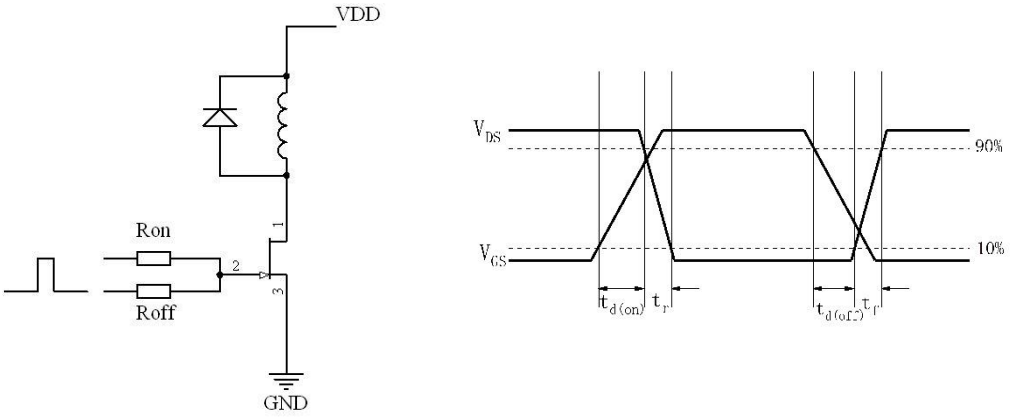
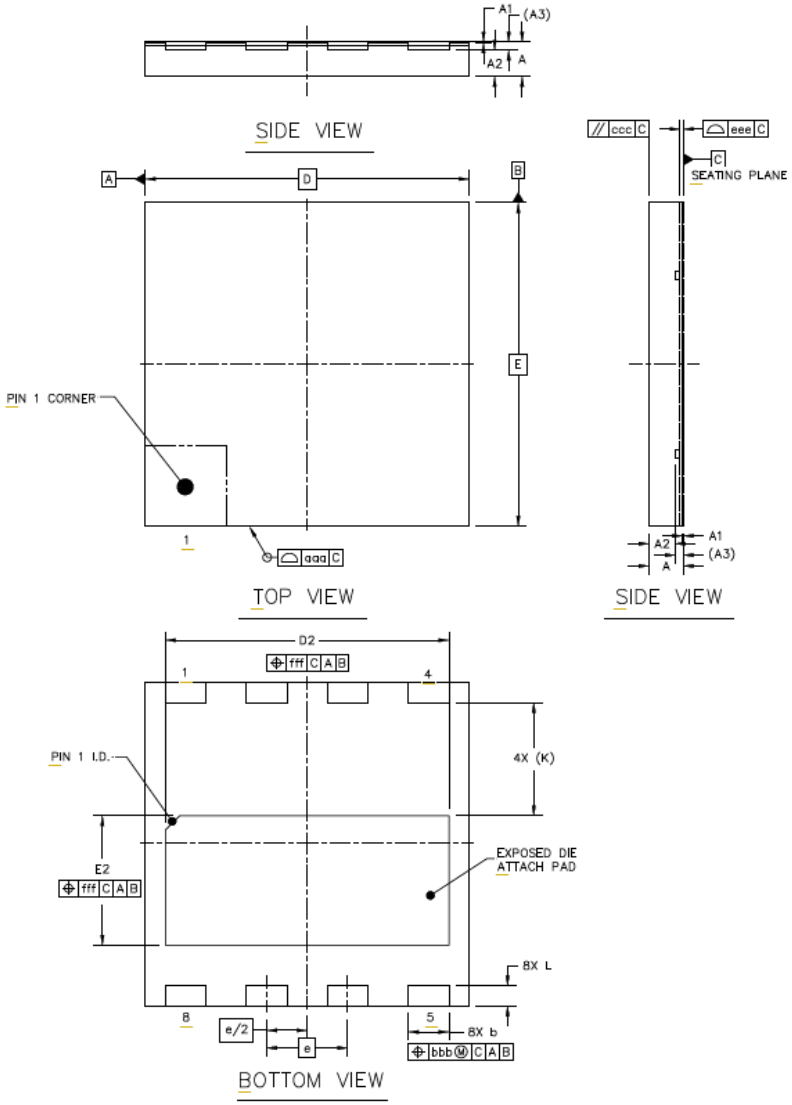


Figure 17. Switching Time Measurement

PQFN8×8 Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.95	1	1.05
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		2 BSC	
EP SIZE	X	D2	6.9	7	7.1
	Y	E2	3.1	3.2	3.3
LEAD LENGTH		L	0.4	0.5	0.6
LEAD TIP TO EXPOSED PAD EDGE		K		2.8 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

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